Physical Product View

Power Requirements

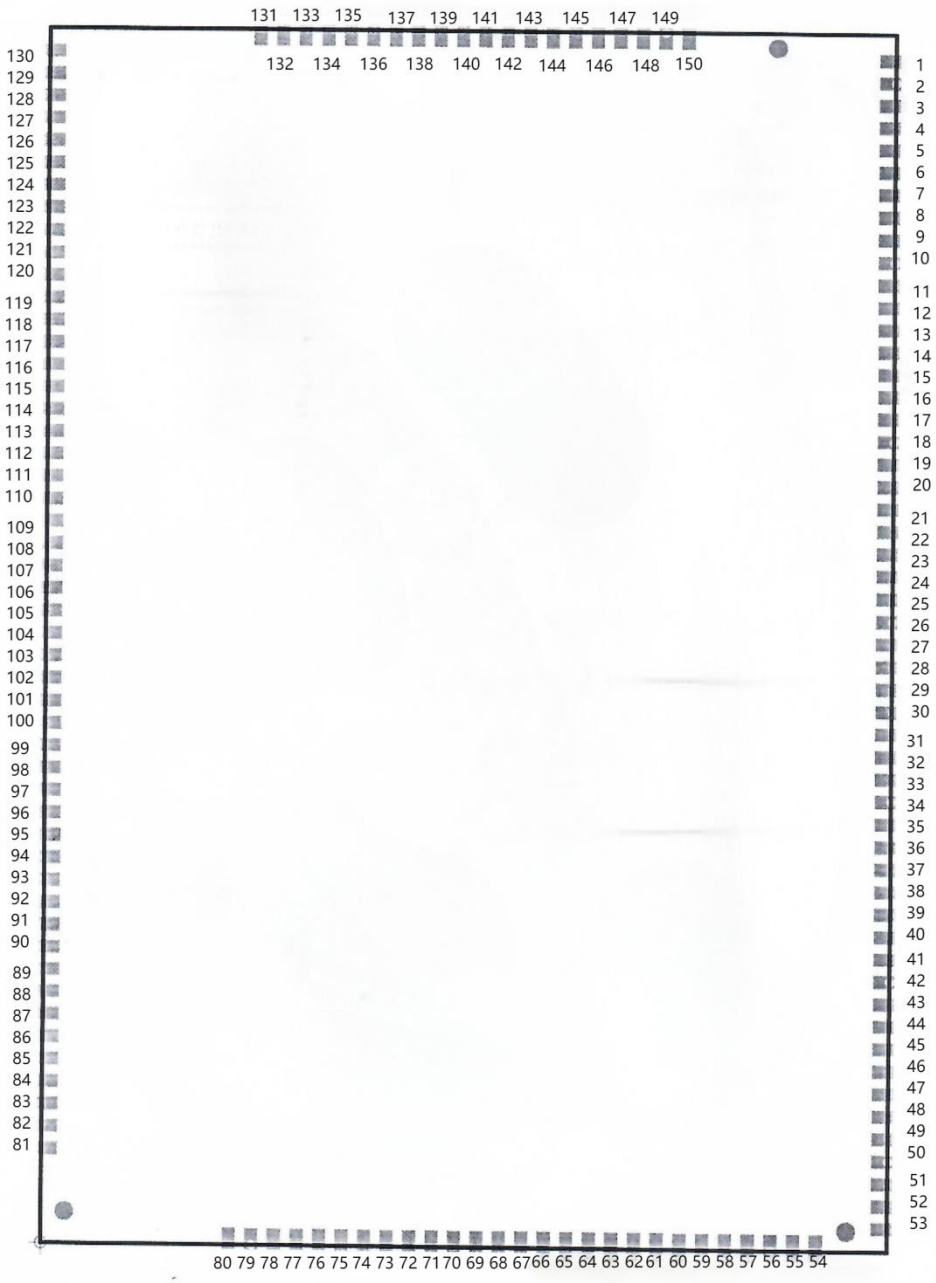
DC Power

Symbol	Parameter	Minimum	Typical	Maximum	Units
DVD3V3	3.3V Supply Voltage	3.13	3.3	3.46	V
DVD12V	12V Supply Voltage	11.40	12.0	12.60	V
DVD5V	5V Supply Voltage	4.75	5.00	5.25	V

Power Consumption

Power Consumption	6W (max)

Pin Assignment



IO Description (PAD)

Symbol	Description
AI	Analog input(does not include pad circuitry)
AO	Analog output(does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input(CMOS)
DO	Digital output(CMOS)
P	Power
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance(high-Z) output

Function Table

TABLE 1 - POWER, GROUND, AND RESET PINS

Pin ID	Pin Name	Type	Description
1, 4, 5, 6, 9, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 49, 51, 53, 55, 57, 59, 75, 76, 77, 78, 79, 80, 81, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 103, 106, 109, 112, 115, 118, 124, 126, 127, 128, 129, 130, 132, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150	GND	GND	Ground
60,82,83	5V_in	I	INPUT 5V
2,3,7,8,56,119,120	DVDD_12V	I	INPUT 12V
10,58	DVDD_1V95	O	OUTPUT 1.95V
137	PQ_RSTIN_N	DI	Hardware reset input

TABLE 2 - PCIe3.0/USB3.0 combo
Option 1 - USB3.0

Pin ID	Pin Name	Type	Description
36	USB0_SS_TXP	AO	Differential output of transmitter
37	USB0_SS_TXN	AO	Differential output of transmitter
39	USBCLKP	AO	Differential reference clock to EP. Frequency = 100 MHz
40	USBCLKN	AO	Differential reference clock to EP. Frequency = 100 MHz
42	USB0_SS_RXP	AI	Differential input of receiver
43	USB0_SS_RXN	AI	Differential input of receiver
45	USB0_DP	AI, AO	USB0 HS data
46	USB0_DM	AI, AO	USB0 HS data

TABLE 2 - PCIe3.0/USB3.0 combo
Option 2 - 1x PCIe3.0 + 1x USB2.0

	Pin ID	Pin Name	Type	Description
PCIe3.0	36	PCIE_TXP	AO	PCIe transmitter differential signal
	37	PCIE_TXN	AO	PCIe transmitter differential signal
	39	PCIE CLKP	AO	Reference clock
	40	PCIE CLKN	AO	Reference clock
	42	PCIE_RXP	AI	PCIe receiver differential signal
	43	PCIE_RXN	AI	PCIe receiver differential signal
USB2.0	Pin ID	Pin Name	Type	Description
	45	USB0_DP	AI, AO	USB0 HS data
	46	USB0_DM	AI, AO	USB0 HS data

Function Table (Continued from Page 3)

TABLE 3 - 2x PCIe 3.0

Pin ID	Pin Name	Type	Description
11	PCIE1_RST_N_5G	B,I	Configurable I/O, also used as PCIE1 PERST
12	PCIE1_WAKE_N_5G	DI	PCIE1 WAKE
13	PCIE1_CLKREQ_N_5G	B	PCIE1 CLKQ
14	PCIE0_WAKE_GPIO45	DI	PCIE2 WAKE
15	PCIE0_RSTN_GPIO44	B,I	Configurable I/O, also used as PCIE2 PERST
16	PCIE0_CLK_REQ_GPIO43	B	PCIE2 CLKQ
18	PCIEX1_TXP1_5G	AO	Dual-lane PCIe PHY transmitter positive output of the first lane
19	PCIEX1_TXN1_5G	AO	Dual-lane PCIe PHY transmitter negative output of the first lane
21	PCIEX1_REFCLK_OP1_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock positive output for the first lane or two-lane mode
22	PCIEX1_REFCLK_ON1_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock negative output for the first-lane or two-lane mode
24	PCIEX1_RXP1_5G	AI	Dual-lane PCIe PHY receiver positive input of the first lane
25	PCIEX1_RXN1_5G	AI	Dual-lane PCIe PHY receiver negative input of the first lane
27	PCIEX2_TXP1_5G	AO	Dual-lane PCIe PHY transmitter positive output of the second lane
28	PCIEX2_TXN1_5G	AO	Dual-lane PCIe PHY transmitter negative output of the second lane
30	PCIEX1_REFCLK_OP2_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock positive output for the second lane
31	PCIEX1_REFCLK_ON2_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock negative output for the second lane
33	PCIEX2_RXP1_5G	AI	Dual-lane PCIe PHY receiver positive input of the second lane
34	PCIEX2_RXN1_5G	AI	Dual-lane PCIe PHY receiver negative input of the second lane
48	WSI_DAT_2>5	B	Wi-Fi MLO data
50	WSI_CLK_2>5	B	Wi-Fi MLO clock
52	WSI_DAT_5>2	B	Wi-Fi MLO DATA
54	WSI_CLK_5>2	B	Wi-Fi MLO clock
61	WDI_GPIO50	B	Wi-Fi WSI data
62	WD_OE_GPIO49	DO	Wi-Fi WSI clock

TABLE 4 - ETHERNET

Pin ID	Pin Name	Type	Description
101	USXGMII_2_TX_N	AO	Differential output of uniphy2 transmitter, support USXGMII/SGMII+/SGMII
102	USXGMII_2_TX_P	AO	Differential output of uniphy2 transmitter, support USXGMII/SGMII+/SGMII
104	SGMII2-_REFCLK	AO	Differential reference clock of uniphy2
105	SGMII2+_REFCLK	AO	Differential reference clock of uniphy2
107	USXGMII_2_RX_N	AI	Differential input of uniphy2 receiver, support USXGMII/SGMII+/SGMII
108	USXGMII_2_RX_P	AI	Differential input of uniphy2 receiver, support USXGMII/SGMII+/SGMI
110	USXGMII_1_TX_N	AO	Differential output of uniphy1 transmitter, support USXGMII/SGMII+/SGMII
111	USXGMII_1_TX_P	AO	Differential output of uniphy1 transmitter, support USXGMII/SGMII+/SGMII
113	USXGMII_1_RX_N	AI	Differential input of uniphy1 receiver, support USXGMII/SGMII+/SGMII
114	USXGMII_1_RX_P	AI	Differential input of uniphy1 receiver, support USXGMII/SGMII+/SGMII
116	SGMII1-_REFCLK	AO	Differential reference clock of uniphy1
117	SGMII1+_REFCLK	AO	Differential reference clock of uniphy1
122	MHT_MDIO	DO	MDIO1
125	MHT_MDC	B	MDC1

GPIO Table

Pin ID	Pad Name	Voltage	Type	GPIO_CFG (FUNC_SEL)	Function	Functional Description
133	GPIO_18	1.8V	B	0	GPIO_IN_OUT(18)	Configurable I/O
			DI	1	BLSP0_UART_RX[0]	UARTO Rx
			DO	2	MAC_SA[0]	MAC smart antenna[0]
134	GPIO_19	1.8V	B	0	GPIO_IN_OUT(19)	Configurable I/O
			DO	1	BLSP0_UART_TX[0]	UARTO Tx
			DO	2	MAC_SA[1]	MAC smart antenna[1]
136	GPIO_20	1.8V	B	0	GPIO_IN_OUT(20)	Configurable I/O
			DO	1	RESOUT	Reset out
135	GPIO_22	1.8V	B	0	GPIO_IN_OUT(22)	Configurable I/O, used as flash reset
123	GPIO_24	1.8V	B	0	GPIO_IN_OUT(24)	Configurable I/O
121	GPIO_25	1.8V	B	0	GPIO_IN_OUT(25)	Configurable I/O
			DI	1	MDC0	MDC0 This interface is used to receive real-time backpressure flow the control message from QCA8386.
			DI	2	BLSP1_UART_RX[1]	UART1 Rx
			B	3	BLSP1_SPI_MOSI[1]	SPI1_MOSI
			DO	4	PWM_OUT3[2]	Pulse Width Modulation interface 3
			DO	5	GPO_CLK[0]	General purpose clock
131	GPIO_26	1.8V	B	0	GPIO_IN_OUT(26)	Configurable I/O
			B	1	MDIO0	MDIO0 This interface is used to receive real-time backpressure flow the control messages from QCA8386.
			DO	2	BLSP1_UART_RFR_N[1]	UART1_RFR_N
			B	3	BLSP1_SPI_CS_N[1]	SPI1 chip select
			DO	4	PWM_OUT2[2]	Pulse Width Modulation interface 2
			DO	5	GP1_CLK[0]	General purpose clock
125	GPIO_27	1.8V	B	0	GPIO_IN_OUT(27)	Configurable I/O
			DO	1	MDC1	MDC1
			DO	2	BLSPO_UART_TX[1]	UARTO Tx
			DO	3	BLSP1_UART_TX[1]	UART1 Tx
			DO	4	BLSP1_SPL_CLK[1]	SPI1 clock
			DO	5	PWM_OUT1[2]	Pulse Width Modulation interface 1
			DO	6	GP2_CLK[0]	General purpose clock
122	GPIO_28	1.8V	B	0	GPIO_IN_OUT(28)	Configurable I/O
			B	1	MDIO1	MDIO1
			DI	2	BLSPO_UART_RX[1]	UART0_RX
			DI	3	BLSP1_UART_CTS_N[1]	UART1 CTS_N
			B	4	BLSP1_SPI_MISO[1]	SPI1 MISO
			DO	5	PWM_OUTO[2]	Pulse Width Modulation interface 0
			DO	7	TSENS_MAX_TEMP_PWM	Temperature sensor PWM
73	GPIO_29	1.8V	B	0	GPIO_IN_OUT(29)	Configurabie I/O
			B	1	AUDIO_PRI_D0	Audio primary port data lane1
			B	2	BLSP1_SPI_MOSI[0]	SPI1 MOSI
			DO	3	BLSP1_12C_SCL[0]	12C1 clock
			DO	4	PWM_OUT3[1]	Pulse Width Modulation interface 3
72	GPIO_30	1.8V	B	0	GPIO_IN_OUT(30)	Configurable I/O
			B	1	AUDIO_PRI_D1	Audio primary port data lane1
			B	2	BLSP1_SPI_CS_N[0]	SPI1 chip select

			B	3	BLSP1_12C_SDA[0]	12C1 SDA
			DO	4	PWM_OUT2[1]	Pulse Width Modulation interface 2
			DO	5	AUDIO_SEC_MCLK_OUT[0]	Audio second port MCLK out
			DI	6	AUDIO_SEC_MCLK_IN[0]	Audio second port MCLK in
70	GPIO_31	1.8V	B	0	GPIO IN_OUT(31)	Configurable I/O
			B	1	AUDIO_PRI_FSYNC	Audio primary port frame sync
			B	2	BLSP1_SPI_MISO[0]	SPI1 MISO
			DO	3	PWM_OUT1[1]	Pulse Width Modulation interface 1
74	GPIO_32	1.8V	B	0	GPIO_IN_OUT(32)	Configurable I/O
			B	1	AUDIO_PRL_PCLK	Audio primary port clock
			DO	2	BLSP1_SPI_CLK[0]	SPI1 clock
			DO	3	PWM_OUTO[1]	Pulse Width Modulation interface 0
71	GPIO_33	1.8V	B	0	GPIO_IN_OUT(33)	Configurable I/O
			B	1	AUDIO_SEC_D0	Audio second port data lane0
			DO	2	BLSP1_UART_TX[2]	UART1 Tx
			DO	3	BLSP2_12C_SCL[1]	12C2 clock
			DO	4	BLSP2_SPI_CLK[0]	SPI2 clock
69	GPIO_34	1.8V	B	0	GPIO_IN_OUT(34)	Configurable I/O
			B	1	AUDIO_SEC_D1	Audio second port data lane1
			DO	2	BLSP1_UART_RFR_N[2]	UART1_RFR_N
			B	3	BLSP2_12C_SDA[1]	2C2_SDA
			B	4	BLSP2_SPI_MOSI[0]	SPI2_MOSI
			DO	5	AUDIO_PRI_MCLK_OUT[0]	Audio primary port MCLK out
			DI	6	AUDIO_PRI_MCLK_IN[0]	Audio primary port MCLK in
65	GPIO_35	1.8V	B	0	GPIO_IN_OUT(35)	Configurable I/O
			B	1	AUDIO_SEC_FSYNC	Audio second port frame sync
			DI	2	BLSP1_UART_RX[2]	UART1 Rx
			B	5	BLSP2_SPI_MISO[0]	SPI2 MISO
67	GPIO_36	1.8V	B	0	GPIO_IN_OUT(36)	Configurable I/O
			B	1	AUDIO_SEC_PCLK	Audio second port PCLK
			DI	2	BLSP1_UART_CTS_N[2]	UART1 CTS_N
			B	5	BLSP2_SPI_CS_N[0]	SPI2 chip select0
68	GPIO_37	1.8V	B	0	GPIO_IN_OUT(37)	Configurable I/O
			B	1	PCIE0_CLK_REQ_N	PCIE0 CLKQ
			B	2	BLSP2_SPI_CS1_N	SPI2 chip select1
64	GPIO_38	1.8V	B	0	GPIO_IN_OUT(38)	Configurable I/O, also used as PCIE0 PERST
66	GPIO_39	1.8V	B	0	GPIO_IN_OUT(39)	Configurable I/O
			DI	1	PCIE0_WAKE	PCIE0 WAKE
54	GPIO_40	1.8V	B	0	GPIO_IN_OUT(40)	Configurable I/O
			DI	1	WSI_CLK_0	Wi-Fi MLO cock
			DO	2	BLSP¹_12C_SCL[1]	12C1 clock
			B	3	BLSP2_SPI_MISO[1]	SPI2 MISO
			DO	4	GP0_CLK[1]	General Purpose clock
52	GPIO_41	1.8V	B	0	GPIO_IN_OUT(41)	Configurable I/O
			B	1	WSL_DATA_0	Wi-Fi MLO DATA
			B	2	BLSP1_12C_SDA[1]	12C1 SDA

			B	3	BLSP2_SPI_MOSI[1]	SPI2 MOSI
			DO	4	GP1_CLK[1]	General Purpose clock
50	GPIO_42	1.8V	B	0	GPIO_IN_OUT(42)	Configurable I/O
			B	1	WSI_CLK_1	Wi-Fi MLO clock
			B	2	BLSP2_SPI_CLK[1]	SPI2_CLK
			DO	3	GP2_CLK[1]	General Purpose clock
16	GPIO_43	1.8V	B	0	GPIO_IN_OUT(43)	Configurable I/O
			B	1	PCIE2_CLK_REQ_N	PCIE2 CLKQ
			B	4	BLSP2_12C_SCL[0]	12C2 SCL
			DO	5	PWM_OUT3[0]	Pulse Width Modulation interface 3
			DO	6	AUDIO_PRI_MCLK_OUT[1]	Audio primary port MCLK out
			DI	7	AUDIO_PRI_MCLK_IN[1]	Audio primary port MCLK in
15	GPIO_44	1.8V	B	0	GPIO_IN_OUT(44)	Configurable I/O, also used as PCIE2 PERST
			DO	1	PWM OUT2[0]	Pulse Width Modulation interface 2
14	GPIO_45	1.8V	B	0	GPIO_IN_OUT(45)	Configurable I/O
			DI	1	PCIE2_WAKE	PCIE2 WAKE
			B	4	BLSP2_12C_SDA[0]	12C2 SDA
			DO	6	PWM_OUT1[0]	Pulse Width Modulation interface 1
			DO	7	AUDIO_SEC_MCLK_OUT[1]	Audio second port MCLK out
			DI	8	AUDIO_SEC_MCLK_IN[1]	Audio second port MCLK in
13	GPIO_46	1.8V	B	0	GPIO_IN_OUT(46)	Configurable I/O
			B	1	PCIE1_CLK DC AI REQ_N	PCIE1 CLKQ
			DO	3	PWM_OUT0[0]	Pulse Width Modulation interface 0
11	GPIO_47	1.8V	B	0	GPIO_IN_OUT(47)	Configurable I/O,also used as PCIE1 PERST
12	GPIO_48	1.8V	B	0	GPIO_IN_OUT(48)	Configurable I/O
			DI	1	PCIE1_WAKE	PCIE1 WAKE
62	GPIO_49	1.8V	B	0	GPIO_IN_OUT(49)	Configurable I/O
			DI	1	PTA_0	Wi-Fi PTA coexist pin, bt_active
			DO	2	CXC_CLK	W-Fi WSI clock
61	GPIO_50	1.8V	B	0	GPIO_IN_OUT(50)	Configurable I/O
			DI	1	PTA_1	Wi-Fi PTA coexist pin, bt_priority
			B	2	CXC_DATA	Wi-Fi WSI data
63	GPIO_51	1.8V	B	0	GPIO_IN_OUT(51)	Configurable I/O
			DO	1	PTA_2	Wi-Fi PTA coexist pin, wl_active
48	GPIO_52	1.8V	B	0	GPIO_IN_OUT(52)	Configurable I/O
			B	1	WSI_DATA_1	Wi-Fi MLO data
			B	2	BLSP2_SPI_CS_N[1]	BLSP2 chip select

PIN STATUS ON BOOT

Pin ID	Pin Name	Type	Description
136	GPIO_20	Boot_Config [3]	Routing refclk control: 0: 48 MHz 1: 96 MHz
135	GPIO_22	Boot_Config [4]	Hash in fuse(software use only): 0: PK hash is stored in boot ROM 1: PK hash is stored in OTP
64	GPIO_38	Boot_Config [6]	Boot ROM boot speed: 0: 24 MHz 1: 400 MHz
50	GPIO_42	Boot_Config [7]	Clock mode select: 0: Master mode 1: Slave mode
15	GPIO_44	Boot_Config [8]	Use Serial Num: 0: Use Serial Num 1: Use OEM ID
11	GPIO_47	Boot_Config [9]	tcxo_mode: 0: xo-mode 1: tcxo-mode
63	GPIO_51	Boot_Config [10]	RFA refclk frequency selection: 0: 48 MHz 1: 96 MHz