



WSB530

Wi-Fi 7 (802.11be) System-on-Module

Hardware User Guide

IPQ5322 Qualcomm Miami Series	2×2 MU-MIMO On-Board 2.4 GHz	Wi-Fi 7 5G Cellular Modules	150-Pin Stamp-Hole SoM
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1. Introduction

Thank you for choosing the Compex WSB530. This document provides complete hardware integration guidance for engineers and system developers deploying the WSB530 System-on-Module (SoM) in custom carrier board designs.

The WSB530 (codename GINGER) is a compact 65 × 45 mm stamp-hole SoM powered by Qualcomm's IPQ5322 'Miami' Series quad-core ARM Cortex-A53 processor. It features an on-board 2×2 2.4 GHz Wi-Fi 7 radio and exposes a rich set of interfaces via its 150-pin edge connector, enabling fully customisable carrier board designs for a wide range of embedded networking applications.

The WSB530 has no on-board physical connectors, buttons, or LEDs. All interfaces — including Ethernet, USB, PCIe, UART, GPIOs, and power rails — are accessible exclusively through the 150-pin stamp-hole edge connector. The end-product form factor, connectivity, and feature set are entirely defined by the customer's carrier board design.

Key Highlights

- Qualcomm IPQ5322 'Miami' Quad-Core ARM Cortex-A53 @ 1.5 GHz SoC.
- On-board 2×2 2.4 GHz MU-MIMO 802.11b/g/n/ax/be radio — up to 688 Mbps; max 22 dBm per chain.
- 1 GB DDR4 RAM (expandable up to 3 GB); 16 GB eMMC flash storage.
- 2× PCIe 3.0 interfaces.
- 1× USB 3.0 (or 1× USB 2.0 + 1× PCIe 3.0 option).
- 3× BLSP ports supporting UART, I2C, and SPI interfaces.
- 33× GPIOs and 4× PWM outputs for carrier board integration.
- 2× U.FL connectors (IPEX1) for on-board 2.4 GHz antenna connection.
- 2× multi-GbE Ethernet SerDes (USXGMII) supporting external 10G/5G/2.5G/1G PHYs.
- Power input via edge connector: 12 V, 5 V, and 3.3 V rails; max 6 W module power.
- 150-pin stamp-hole edge connector for carrier board integration.
- CE Certified, REACH & RoHS Compliant.

Intended Use

The WSB530 is a SoM intended exclusively for integration onto a custom carrier board. It is not a standalone product and requires a carrier board designed to the WSB530 interface specifications to function. Typical target applications include:

- 802.11be MU-MIMO OFDMA wireless access points.
- IoT gateways and edge computing nodes.
- Industrial networking appliances and custom embedded systems.
- Any application requiring a customised form factor, interface selection, and feature set.

2. Package Contents

Verify the following items are included in the package before proceeding with installation:

Checklist

- 1 × WSB530 System-on-Module

⚠ Note: The WSB530 is a bare SoM. No carrier board, antennas, power supply, cables, or accessories are included. All end-product integration components must be provided by the customer. Contact sales@compex.com.sg for accessory options.

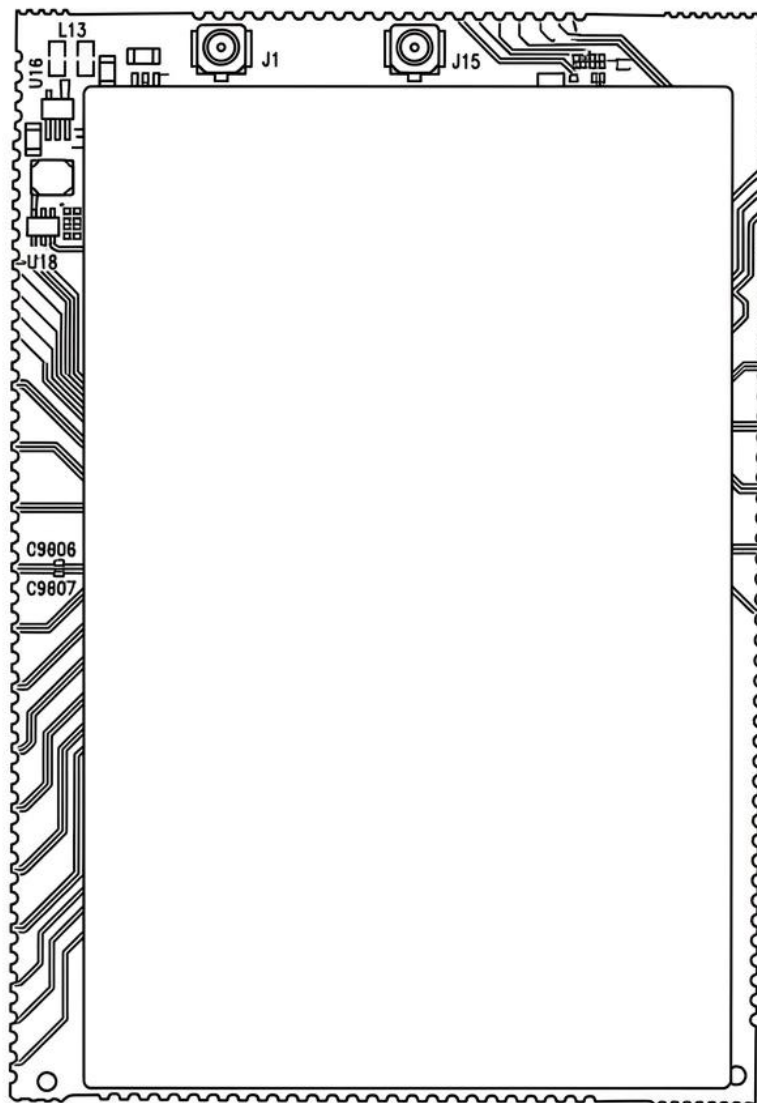
If any item is missing or damaged, contact Compex Technical Support (see Chapter 11) before proceeding.

3. Hardware Overview

The WSB530 is a 65 × 45 × 7.4 mm stamp-hole SoM. All interfaces are exposed via a 150-pin edge connector on the underside of the module. The top side of the module carries the SoC, DDR4 memory, eMMC flash, and the 2.4 GHz radio with its 2× U.FL antenna connectors.

3.1 Module Layout

The following table summarises the main components and available interfaces of the WSB530:



SoC	Qualcomm IPQ5322 'Miami' Series, Quad-Core ARM Cortex-A53 @ 1.5 GHz
Reference Design	Qualcomm AP.MI01.2
System Memory	1 GB DDR4 (up to 3 GB), 16-bit interface (1× 16-bit)
Flash Storage	No NOR Flash; eMMC: 16 GB
On-Board Wi-Fi	2×2 2.4 GHz MU-MIMO 802.11b/g/n/ax/be, max 22 dBm per chain
RF Connectors	2× U.FL (IPEX1) — only physical connectors on the WSB530 module; for 2.4 GHz antenna (CH0, CH1)
PCIe 3.0	2× PCIe 3.0
USB	1× USB 3.0 (or 1× USB 2.0 + 1L PCIe 3.0 option)
BLSP / Serial	3× BLSP ports for UART, I2C, and SPI
GPIOs	33× GPIOs
PWM	4× PWM outputs
Ethernet	2× multi-GbE Ethernet SerDes (USXGMII); external PHY required on carrier board
Edge Connector	150-pin stamp-hole connector — primary interface between WSB530 and carrier board; all signals (PCIe, USB, Ethernet, GPIOs, UART, power) are routed through this connector
Reset	Via voltage monitor; PQ_RSTIN_N available at pin 137
Dimensions (W×H×D)	65 mm × 45 mm × 7.4 mm, stamp-hole SoM

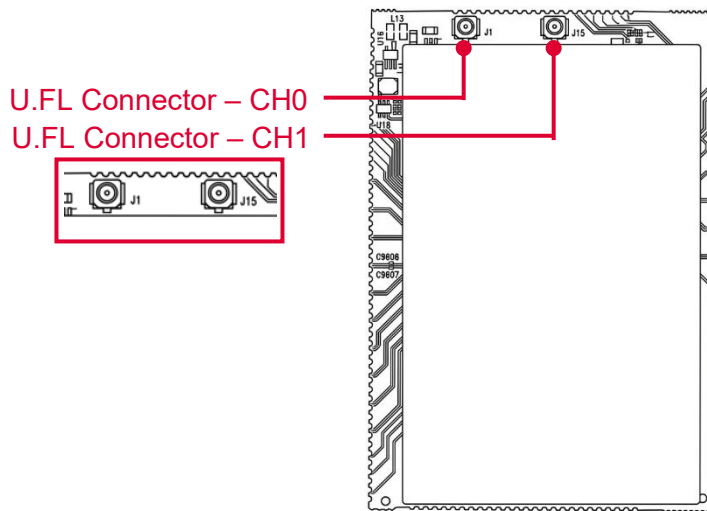
⚠ Note: All interfaces listed above are available via the 150-pin edge connector only. The WSB530 itself has no physical ports, buttons, or LED indicators. These must be implemented on the customer carrier board.

3.2 Connector Descriptions

The WSB530 is a 65 × 45 × 7.4 mm stamp-hole SoM. All interfaces are exposed via a 150-pin edge connector on the underside of the module. The top side of the module carries the SoC, DDR4 memory, eMMC flash, and the 2.4 GHz radio with its 2× U.FL antenna connectors.

2.4 GHz U.FL Antenna Connectors (On-Module)

- 2× U.FL (IPEX1) connectors are the only physical connectors on the WSB530 module itself.
- Connect 2× antennas (50 Ω, rated for 2.4 GHz) to CH0 and CH1 before powering on.
- For 5 GHz / 6 GHz radio operation via modules on the carrier board, antenna connections are implemented on the carrier board.



PCIe 3.0

- 2× PCIe 3.0 interfaces available via edge connector.
- Supports Wi-Fi 7 radio modules and 5G cellular modules via PCIe 3.0.

PWM

- 4× PWM outputs available via GPIOs for fan control, LED dimming, or other carrier board functions.

Reset

- Reset is controlled via an on-module voltage monitor. No physical reset button is present on the WSB530.
- Carrier board designers may implement an external reset circuit connected to the PQ_RSTIN_N signal.

USB

- Option 1 (USB 3.0 mode): 1× USB 3.0 interface.
- Option 2 (USB 2.0 + PCIe mode): 1× USB 2.0 + 1L PCIe 3.0 interface.
- USB mode is controlled by the Force USB Switch signal. Carrier board should expose this appropriately (ON = Normal mode, OFF = Force USB).

BLSP / Serial Interfaces

- 3× BLSP ports supporting UART, I2C, and SPI — available via edge connector GPIO pins.
- UART: used for serial console access. Carrier board should expose a debug header (4-pin TTL or RS-232 via converter).
- I2C and SPI: available for peripheral device integration on the carrier board.

Ethernet SerDes

- 2× multi-GbE Ethernet SerDes (USXGMII).
- Requires an external Ethernet PHY chip on the carrier board (supporting 10G, 5G, 2.5G, or 1G operation).
- SGMII reference clocks also available for alternative PHY configurations.
- Carrier board Ethernet connector type (RJ45, SFP, etc.) is entirely designer's choice.

GPIOs

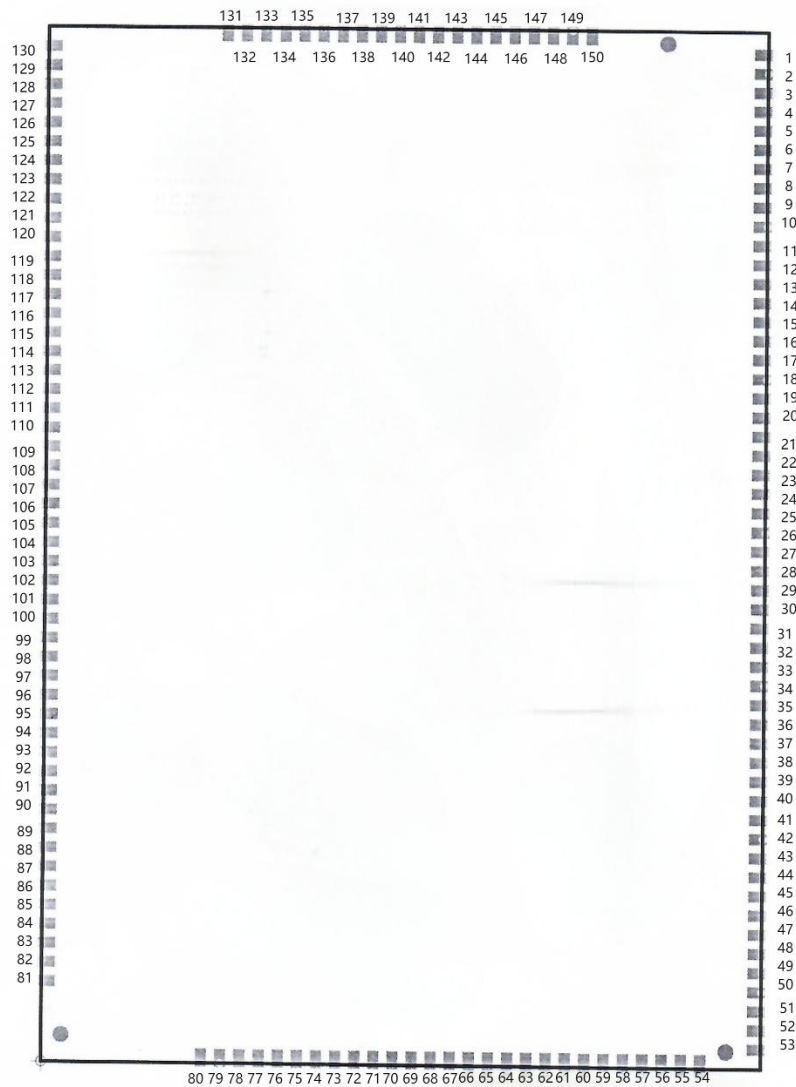
- 33× GPIOs available via edge connector for carrier board use.
- Functions include: LED control outputs, NAND flash control, SPI, PCIe control signals, and general I/O.
- See Section 3.3 for full GPIO mapping.

Power Rails

- The WSB530 requires 3 power rails supplied from the carrier board: DVDD_12V (12 V), 5V_in (5 V), DVDD_3V3 (3.3 V).
- All three rails must be supplied simultaneously and stable before the module powers on correctly.
- Note: DVDD_1V95 is a 1.95 V reference voltage generated and output by the module — it is not a carrier board input rail and does not need to be supplied externally.
- See Section 6 for power specifications and Section 7.2 for carrier board power design guidelines.

3.3 Hardware Pinouts

The following tables list the complete 150-pin edge connector assignment for the WSB530. All interfaces to the carrier board are via this connector.



Pin Assignment — Pin 1 to 80

Pin ID	Pin Name	Pin ID	Pin Name
1	GND	41	GND
2	DVDD_12V	42	USB0_SS_RXP (Opt1-USB3.0) / PCIE_RXP (Opt2)
3	DVDD_12V	43	USB0_SS_RXN (Opt1-USB3.0) / PCIE_RXN (Opt2)
4	GND	44	GND
5	GND	45	USB0_DP
6	GND	46	USB0_DM
7	DVDD_12V	47	GND
8	DVDD_12V	48	WSI_DAT_2>5
9	GND	49	GND
10	DVDD_1V95	50	WSI_CLK_2>5 / GPIO42
11	PCIE1_RST_N_5G / GPIO_20	51	GND
12	PCIE1_WAKE_N_5G	52	WSI_DAT_5>2
13	PCIE1_CLKREQ_N_5G	53	GND
14	PCIE0_WAKE_GPIO45	54	WSI_CLK_5>2
15	PCIE0_RSTN_GPIO44	55	GND
16	PCIE0_CLK_REQ_GPIO43	56	DVDD_12V
17	GND	57	GND
18	PCIEX1_TXP1_5G	58	DVDD_1V95
19	PCIEX1_TXN1_5G	59	GND
20	GND	60	5V_in
21	PCIEX1_REFCLK_OP1_5G	61	WDI_GPIO50
22	PCIEX1_REFCLK_ON1_5G	62	WD_OE_GPIO49
23	GND	63	GPIO_51
24	PCIEX1_RXP1_5G	64	GPIO_38
25	PCIEX1_RXN1_5G	65	GPIO_35
26	GND	66	GPIO_39
27	PCIEX2_TXP1_5G	67	GPIO_36
28	PCIEX2_TXN1_5G	68	GPIO_37
29	GND	69	GPIO_34
30	PCIEX1_REFCLK_OP2_5G	70	GPIO_31
31	PCIEX1_REFCLK_ON2_5G	71	GPIO_33
32	GND	72	GPIO_30
33	PCIEX2_RXP1_5G	73	GPIO_29
34	PCIEX2_RXN1_5G	74	GPIO_32
35	GND	75	GND
36	USB0_SS_TXP (Opt1) / PCIE_TXP (Opt2)	76	GND
37	USB0_SS_TXN (Opt1) / PCIE_TXN (Opt2)	77	GND
38	GND	78	GND
39	USBCLKP (Opt1) / PCIE_CLKP (Opt2)	79	GND
40	USBCLKN (Opt1) / PCIE_CLKN (Opt2)	80	GND

Pin Assignment — Pin 81 to 150

Pin ID	Pin Name	Pin ID	Pin Name
81	GND	116	SGMII1-_REFCLK
82	5V_in	117	SGMII1+_REFCLK
83	5V_in	118	GND
84	GND	119	DVDD_12V
85	GND	120	DVDD_12V
86	GND	121	GPIO_25
87	GND	122	MHT_MDIO / GPIO_28
88	GND	123	GPIO_24
89	GND	124	GND
90	GND	125	MHT_MDC / GPIO_27
91	GND	126	GND
92	GND	127	GND
93	GND	128	GND
94	GND	129	GND
95	GND	130	GND
96	GND	131	GPIO_26
97	GND	132	GND
98	GND	133	GPIO_18
99	GND	134	GPIO_19
100	GND	135	GPIO_22
101	USXGMII_2_TX_N	136	GPIO_20
102	USXGMII_2_TX_P	137	PQ_RSTIN_N
103	GND	138	GND
104	SGMII2-_REFCLK	139	GND
105	SGMII2+_REFCLK	140	GND
106	GND	141	GND
107	USXGMII_2_RX_N	142	GND
108	USXGMII_2_RX_P	143	GND
109	GND	144	GND
110	USXGMII_1_TX_N	145	GND
111	USXGMII_1_TX_P	146	GND
112	GND	147	GND
113	USXGMII_1_RX_N	148	GND
114	USXGMII_1_RX_P	149	GND
115	GND	150	GND

IO Description (PAD)

Pin	Signal
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
P	Power
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance(high-Z) output

Function Table

Table 1 – Power, Ground, And Reset Pins

Pin ID	Pin Name	Type	Description
1, 4, 5, 6, 9, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 49, 51, 53, 55, 57, 59, 75, 76, 77, 78, 79, 80, 81, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 103, 106, 109, 112, 115, 118, 124, 126, 127, 128, 129, 130, 132, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150	GND	GND	Ground
60,82,83	5V_in	I	INPUT 5V
2,3,7,8,56,119,120	DVDD_12V	I	INPUT 12V
10,58	DVDD_1V95	O	OUTPUT 1.95V
137	PQ_RSTIN_N	DI	Hardware reset input

Table 2 – PCIe3.0/USB3.0 combo

Option 1 – USB3.0

Pin ID	Pin Name	Type	Description
36	USB0_SS_TXP	AO	Differential output of transmitter
37	USB0_SS_TXN	AO	Differential output of transmitter
39	USBCLKP	AO	Differential reference clock to EP. Frequency = 100 MHz
40	USBCLKN	AO	Differential reference clock to EP. Frequency = 100 MHz
42	USB0_SS_RXP	AI	Differential input of receiver
43	USB0_SS_RXN	AI	Differential input of receiver
45	USB0_DP	AI, AO	USB0 HS data
46	USB0_DM	AI, AO	USB0 HS data

Table 2 – PCIe3.0/USB3.0 combo

Option 2 – 1x PCIe3.0 + 1x USB2.0

PCIe3.0	Pin ID	Pin Name	Type	Description
	36	USB0_SS_TXP	AO	Differential output of transmitter
	37	USB0_SS_TXN	AO	Differential output of transmitter
	39	USBCLKP	AO	Differential reference clock to EP. Frequency = 100 MHz
	40	USBCLKN	AO	Differential reference clock to EP. Frequency = 100 MHz
	42	USB0_SS_RXP	AI	Differential input of receiver
USB2.0	43	USB0_SS_RXN	AI	Differential input of receiver
	Pin ID	Pin Name	Type	Description
	45	USB0_DP	AI, AO	USB0 HS data
	46	USB0_DM	AI, AO	USB0 HS data

Table 3 – Ethernet

Pin ID	Pin Name	Type	Description
101	USXGMII_2_TX_N	AO	Differential output of uniphy2 transmitter, support USXGMII/SGMII+/SGMII
102	USXGMII_2_TX_P	AO	Differential output of uniphy2 transmitter, support USXGMII/SGMII+/SGMII
104	SGMII2-_REFCLK	AO	Differential reference clock of uniphy2
105	SGMII2+_REFCLK	AO	Differential reference clock of uniphy2
107	USXGMII_2_RX_N	AI	Differential input of uniphy2 receiver, support USXGMII/SGMII+/SGMII
108	USXGMII_2_RX_P	AI	Differential input of uniphy2 receiver, support USXGMII/SGMII+/SGMII
110	USXGMII_1_TX_N	AO	Differential output of uniphy1 transmitter, support USXGMII/SGMII+/SGMII
111	USXGMII_1_TX_P	AO	Differential output of uniphy1 transmitter, support USXGMII/SGMII+/SGMII
113	USXGMII_1_RX_N	AI	Differential input of uniphy1 receiver, support USXGMII/SGMII+/SGMII
114	USXGMII_1_RX_P	AI	Differential input of uniphy1 receiver, support USXGMII/SGMII+/SGMII
116	SGMII1-_REFCLK	AO	Differential reference clock of uniphy1
117	SGMII1+_REFCLK	AO	Differential reference clock of uniphy1
122	MHT_MDIO	DO	MDIO1
125	MHT_MDC	B	MDC1

Table 4 – 2x PCIe3.0

Pin ID	Pin Name	Type	Description
11	PCIE1_RST_N_5G	B,I	Configurable I/O, also used as PCIE1
12	PCIE1_WAKE_N_5G	DI	PCIE1 WAKE
13	PCIE1_CLKREQ_N_5G	B	PCIE1 CLKQ
14	PCIE0_WAKE_GPIO45	DI	PCIE2 WAKE
15	PCIE0_RSTN_GPIO44	B,I	Configurable I/O, also used as PCIE2
16	PCIE0_CLK_REQ_GPIO43	B	PCIE2 CLKQ
18	PCIEX1_TXP1_5G	AO	Dual-lane PCIe PHY transmitter positive output of the first lane
19	PCIEX1_TXN1_5G	AO	Dual-lane PCIe PHY transmitter negative output of the first lane
21	PCIEX1_REFCLK_OP1_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock positive output for the first lane or two-lane mode
22	PCIEX1_REFCLK_ON1_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock negative output for the first-lane or two-lane mode
24	PCIEX1_RXP1_5G	AI	Dual-lane PCIe PHY receiver positive input of the first lane
25	PCIEX1_RXN1_5G	AI	Dual-lane PCIe PHY receiver negative input of the first lane
27	PCIEX2_TXP1_5G	AO	Dual-lane PCIe PHY transmitter positive output of the second lane
28	PCIEX2_TXN1_5G	AO	Dual-lane PCIe PHY transmitter negative output of the second lane
30	PCIEX1_REFCLK_OP2_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock positive output for the second lane
31	PCIEX1_REFCLK_ON2_5G	AO	Dual-lane PCIe PHY differential 100 MHz reference clock negative output for the second lane
33	PCIEX2_RXP1_5G	AI	Dual-lane PCIe PHY receiver positive input of the second lane
34	PCIEX2_RXN1_5G	AI	Dual-lane PCIe PHY receiver negative input of the second lane
48	WSI_DAT_2>5	B	Wi-Fi MLO data
50	WSI_CLK_2>5	B	Wi-Fi MLO clock
52	WSI_DAT_5>2	B	Wi-Fi MLO DATA
54	WSI_CLK_5>2	B	Wi-Fi MLO clock
61	WDI_GPIO50	B	Wi-Fi WSI data
62	WD_OE_GPIO49	DO	Wi-Fi WSI clock

GPIO Table

Pin ID	Pad Name	Voltage	Type	GPIO_CFG (FUNC_SEL)	Function	Functional Description
133	GPIO_18	1.8V	B	0	GPIO_IN_OUT(18)	Configurable I/O
			DI	1	BLSP0_UART_RX[0]	UART0 Rx
			DO	2	MAC_SA[0]	MAC smart antenna[0]
134	GPIO_19	1.8V	B	0	GPIO_IN_OUT(19)	Configurable I/O
			DO	1	BLSP0_UART_TX[0]	UART0 Tx
			DO	2	MAC_SA[1]	MAC smart antenna[1]
136	GPIO_20	1.8V	B	0	GPIO_IN_OUT(20)	Configurable I/O
			DO	1	RESOUT	Reset out
135	GPIO_22	1.8V	B	0	GPIO_IN_OUT(22)	Configurable I/O, used as flash reset
123	GPIO_24	1.8V	B	0	GPIO_IN_OUT(24)	Configurable I/O
121	GPIO_25	1.8V	B	0	GPIO_IN_OUT(25)	Configurable I/O
			DI	1	MDC0	MDC0 This interface is used to receive real-time backpressure flow the control message from QCA8386.
			DI	2	BLSP1_UART_RX[1]	UART1 Rx
			B	3	BLSP1_SPI_MOSI[1]	SPI1_MOSI
			DO	4	PWM_OUT3[2]	Pulse Width Modulation interface 3
			DO	5	GPO_CLK[0]	General purpose clock
131	GPIO_26	1.8V	B	0	GPIO_IN_OUT(26)	Configurable I/O
			B	1	MDIO0	MDIO0 This interface is used to receive real-time backpressure flow the control messages from QCA8386.
			DO	2	BLSP1_UART_RFR_N[1]	UART1_RFR_N
			B	3	BLSP1_SPI_CS_N[1]	SPI1 chip select
			DO	4	PWM_OUT2[2]	Pulse Width Modulation interface 2

			DO	5	GP1_CLK[0]	General purpose clock
125	GPIO_27	1.8V	B	0	GPIO_IN_OUT(27)	Configurable I/O
			DO	1	MDC1	MDC1
			DO	2	BLSP0_UART_TX[1]	UART0 Tx
			DO	3	BLSP1_UART_TX[1]	UART1 Tx
			DO	4	BLSP1_SPL_CLK[1]	SPI1 clock
			DO	5	PWM_OUT1[2]	Pulse Width Modulation interface 1
			DO	6	GP2_CLK[0]	General purpose clock
122	GPIO_28	1.8V	B	0	GPIO_IN_OUT(28)	Configurable I/O
			B	1	MDIO1	MDIO1
			DI	2	BLSP0_UART_RX[1]	UART0_RX
			DI	3	BLSP1_UART_CTS_N[1]	UART1 CTS_N
			B	4	BLSP1_SPI_MISO[1]	SPI1 MISO
			DO	5	PWM_OUT0[2]	Pulse Width Modulation interface 0
			DO	7	TSENS_MAX_TEMP_PWM	Temperature sensor PWM
73	GPIO_29	1.8V	B	0	GPIO_IN_OUT(29)	Configurable I/O
			B	1	AUDIO_PRI_D0	Audio primary port data lane1
			B	2	BLSP1_SPI_MOSI[0]	SPI1 MOSI
			DO	3	BLSP1_12C_SCL[0]	12C1 clock
			DO	4	PWM_OUT3[1]	Pulse Width Modulation interface 3
72	GPIO_30	1.8V	B	0	GPIO_IN_OUT(30)	Configurable I/O
			B	1	AUDIO_PRI_D1	Audio primary port data lane1
			B	2	BLSP1_SPI_CS_N[0]	SPI1 chip select
			B	3	BLSP1_12C_SDA[0]	12C1 SDA
			DO	4	PWM_OUT2[1]	Pulse Width Modulation interface 2

			DO	5	AUDIO_SEC_MCLK_OUT[0]	Audio second port MCLK out
			DI	6	AUDIO_SEC_MCLK_IN[0]	Audio second port MCLK in
70	GPIO_31	1.8V	B	0	GPIO_IN_OUT(31)	Configurable I/O
			B	1	AUDIO_PRI_FSYNC	Audio primary port frame sync
			B	2	BLSP1_SPI_MISO[0]	SPI1 MISO
			DO	3	PWM_OUT1[1]	Pulse Width Modulation interface 1
74	GPIO_32	1.8V	B	0	GPIO_IN_OUT(32)	Configurable I/O
			B	1	AUDIO_PRL_PCLK	Audio primary port clock
			DO	2	BLSP1_SPI_CLK[0]	SPI1 clock
			DO	3	PWM_OUT0[1]	Pulse Width Modulation interface 0
71	GPIO_33	1.8V	B	0	GPIO_IN_OUT(33)	Configurable I/O
			B	1	AUDIO_SEC_DATA0	Audio second port data lane0
			DO	2	BLSP1_UART_TX[2]	UART1 Tx
			DO	3	BLSP2_12C_SCL[1]	12C2 clock
			DO	4	BLSP2_SPI_CLK[0]	SPI2 clock
69	GPIO_34	1.8V	B	0	GPIO_IN_OUT(34)	Configurable I/O
			B	1	AUDIO_SEC_DATA1	Audio second port data lane1
			DO	2	BLSP1_UART_RFR_N[2]	UART1_RFR_N
			B	3	BLSP2_12C_SDA[1]	2C2_SDA
			B	4	BLSP2_SPI_MOSI[0]	SPI2_MOSI
			DO	5	AUDIO_PRI_MCLK_OUT[0]	Audio primary port MCLK out
			DI	6	AUDIO_PRI_MCLK_IN[0]	Audio primary port MCLK in
65	GPIO_35	1.8V	B	0	GPIO_IN_OUT(35)	Configurable I/O
			B	1	AUDIO_SEC_FRAME_SYNC	Audio second port frame sync

			DI	2	BLSP1_UART_RX[2]	UART1 Rx
			B	5	BLSP2_SPI_MISO[0]	SPI2 MISO
67	GPIO_36	1.8V	B	0	GPIO_IN_OUT(36)	Configurable I/O
			B	1	AUDIO_SEC_PCLK	Audio second port PCLK
			DI	2	BLSP1_UART_CTS_N[2]	UART1 CTS_N
			B	5	BLSP2_SPI_CS_N[0]	SPI2 chip select0
68	GPIO_37	1.8V	B	0	GPIO_IN_OUT(37)	Configurable I/O
			B	1	PCIE0_CLK_REQ_N	PCIE0 CLKQ
			B	2	BLSP2_SPI_CS1_N	SPI2 chip select1
64	GPIO_38	1.8V	B	0	GPIO_IN_OUT(38)	Configurable I/O, also used as PCIE0 PERST
66	GPIO_39	1.8V	B	0	GPIO_IN_OUT(39)	Configurable I/O
			DI	1	PCIE0_WAKE	PCIE0 WAKE
54	GPIO_40	1.8V	B	0	GPIO_IN_OUT(40)	Configurable I/O
			DI	1	WSI_CLK_0	Wi-Fi MLO clock
			DO	2	BLSP1_I2C_SCL[1]	12C1 clock
			B	3	BLSP2_SPI_MISO[1]	SPI2 MISO
			DO	4	GP0_CLK[1]	General Purpose clock
52	GPIO_41	1.8V	B	0	GPIO_IN_OUT(41)	Configurable I/O
			B	1	WSL_DATA_0	Wi-Fi MLO DATA
			B	2	BLSP1_I2C_SDA[1]	12C1 SDA
			B	3	BLSP2_SPI_MOSI[1]	SPI2 MOSI
			DO	4	GP1_CLK[1]	General Purpose clock
50	GPIO_42	1.8V	B	0	GPIO_IN_OUT(42)	Configurable I/O
			B	1	WSI_CLK_1	Wi-Fi MLO clock
			B	2	BLSP2_SPI_CLK[1]	SPI2_CLK

			DO	3	GP2_CLK[1]	General Purpose clock
16	GPIO_43	1.8V	B	0	GPIO_IN_OUT(43)	Configurable I/O
			B	1	PCIE2_CLK_REQ_N	PCIE2 CLKQ
			B	4	BLSP2_12C_SCL[0]	12C2 SCL
			DO	5	PWM_OUT3[0]	Pulse Width Modulation interface 3
			DO	6	AUDIO_PRI_MCLK_OUT[1]	Audio primary port MCLK out
			DI	7	AUDIO_PRI_MCLK_IN[1]	Audio primary port MCLK in
15	GPIO_44	1.8V	B	0	GPIO_IN_OUT(44)	Configurable I/O, also used as PCIE2 PERST
			DO	1	PWM_OUT2[0]	Pulse Width Modulation interface 2
14	GPIO_45	1.8V	B	0	GPIO_IN_OUT(45)	Configurable I/O
			DI	1	PCIE2_WAKE	PCIE2 WAKE
			B	4	BLSP2_12C_SDA[0]	12C2 SDA
			DO	6	PWM_OUT1[0]	Pulse Width Modulation interface 1
			DO	7	AUDIO_SEC_MCLK_OUT[1]	Audio second port MCLK out
			DI	8	AUDIO_SEC_MCLK_IN[1]	Audio second port MCLK in
13	GPIO_46	1.8V	B	0	GPIO_IN_OUT(46)	Configurable I/O
			B	1	PCIE1_CLK_DC_AI_REQ_N	PCIE1 CLKQ
			DO	3	PWM_OUT0[0]	Pulse Width Modulation interface 0
11	GPIO_47	1.8V	B	0	GPIO_IN_OUT(47)	Configurable I/O, also used as PCIE1 PERST
12	GPIO_48	1.8V	B	0	GPIO_IN_OUT(48)	Configurable I/O
			DI	1	PCIE1_WAKE	PCIE1 WAKE
62	GPIO_49	1.8V	B	0	GPIO_IN_OUT(49)	Configurable I/O
			DI	1	PTA_0	Wi-Fi PTA coexist pin, bt_active
			DO	2	CXC_CLK	W-Fi WSI clock

61	GPIO_50	1.8V	B	0	GPIO_IN_OUT(50)	Configurable I/O
			DI	1	PTA_1	Wi-Fi PTA coexist pin, bt_priority
			B	2	CXC_DATA	Wi-Fi WSI data
63	GPIO_51	1.8V	B	0	GPIO_IN_OUT(51)	Configurable I/O
			DO	1	PTA_2	Wi-Fi PTA coexist pin, wl_active
48	GPIO_52	1.8V	B	0	GPIO_IN_OUT(52)	Configurable I/O
			B	1	WSI_DATA_1	Wi-Fi MLO data
			B	2	BLSP2_SPI_CS_N[1]	BLSP2 chip select

4. Radio Module Specifications

4.1 Wi-Fi Capability

The WSB530 features an on-board 2×2 2.4 GHz MU-MIMO Wi-Fi 7 radio driven by the Qualcomm IPQ5322 SoC. For 5 GHz or 6 GHz Wi-Fi operation, a compatible PCIe Wi-Fi radio module must be integrated on the carrier board and connected to the WSB530's PCIe 3.0 interface via the edge connector.

Wi-Fi Standard	IEEE 802.11be (Wi-Fi 7) — backward compatible to 802.11a/b/g/n/ac/ax
2.4 GHz Radio (On-Module)	2×2 MU-MIMO 802.11b/g/n/ax/be; up to 688 Mbps; max 22 dBm per chain
5 GHz / 6 GHz Radio	Supports Wi-Fi 7 and 5G cellular modules
Frequency Range	2.4 GHz: 2.412–2.472 GHz
Channel Widths	2.4 GHz: 20/40 MHz (EHT20 / EHT40)
Modulation	OFDMA: BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM, 4096-QAM
RF Connectors	2× U.FL (IPEX1) on-module connectors for 2.4 GHz (CH0 & CH1)
Security	WPA3-Personal, WPA3-Enterprise, OWE, WPA2 (backward compatible)
Operating Modes	AP, Station (Client)

4.2 Notes & Recommendations

- Connect antennas to both U.FL ports (CH0, CH1) before powering on. Never operate with open U.FL connectors.
- Supports Wi-Fi 7 and 5G cellular modules via PCIe 3.0 on the carrier board.
- For 6 GHz band operation, verify local regulatory approval in the target market before deployment.
- Use 50 Ω impedance-matched antennas for all radio frequency bands.
- Wi-Fi performance depends on antenna design, carrier board layout, channel configuration, and environmental conditions. Consult Compex for antenna and RF design recommendations.

5. Mechanical Specifications

5.1 Module Dimensions

Overall Dimensions (W × H × D)	65 mm × 45 mm × 7.4 mm
Form Factor	Stamp-hole SoM, 150-pin edge connector on underside
PCB Layer Count	Multi-layer PCB
Mounting Method	Solder or press-fit onto carrier board via 150-pin stamp-hole pads

5.2 Environmental Ratings

Operating Humidity	5% to 95% (non-condensing)
Storage Humidity	Max. 90% (non-condensing)
Certification	CE Certified, REACH & RoHS Compliant

6. Power Specifications

6.1 Power Requirements

The WSB530 is powered entirely via the 150-pin edge connector. Three power rails must be supplied from the carrier board:

Input Voltage	3.3V, 5V, 12V
Power Consumption (Module only, Max)	6 W

6.2 Power Delivery Protection

- Carrier board power supply design must account for module peak current demand plus any additional carrier board loads (PHY, radio modules, etc.).
- Use local bypass capacitors on all power rail pads of the edge connector on the carrier board.
- Implement appropriate power sequencing if required by the carrier board's power architecture.
- Never exceed the rated input voltages. Overvoltage on any rail may permanently damage the module.

7. Integration Guidelines

This section provides hardware design guidelines for integrating the WSB530 onto a custom carrier board. These are recommendations based on Qualcomm IPQ5322 design requirements and Compex engineering experience.

7.1 Power Rail Design

- Use low-noise switching regulators with sufficient output current capacity for each rail.
- Place input and output bulk capacitors close to regulator ICs, and place 100 nF ceramic bypass capacitors on each power pad of the WSB530 edge connector footprint.
- Ensure power planes are solid and well-connected under the WSB530 footprint with adequate via stitching.
- Implement OVP (Over-Voltage Protection) and OCP (Over-Current Protection) on all input rails to protect the module.

7.2 High-Speed Signal Routing

- USXGMII Ethernet SerDes: Route as 100 Ω differential pairs. Keep traces short, length-matched, and avoid vias where possible. Place the Ethernet PHY as close as possible to the WSB530 edge connector footprint.
- PCIe 3.0: Route as 85 Ω differential pairs. Maintain length matching within each differential pair (< 5 mil skew) and between TX/RX pairs (< 20 mil). Place AC coupling capacitors (100 nF) in series on TX lines.
- USB 3.0: Route as 90 Ω differential pairs. Keep traces away from noisy switching signals.
- Avoid routing high-speed differential pairs under or near the WSB530 module.
- All GND pins of the edge connector must be connected to a solid ground plane with low inductance vias.

7.3 Antenna Design

- For on-module 2.4 GHz radio: connect external antennas via U.FL cables to CH0 and CH1 on the WSB530. Antenna cables should be kept as short as possible.
- For 5 GHz / 6 GHz radio modules on the carrier board: route antenna connections per the radio module's design guide. Ensure antenna placement provides adequate isolation from the 2.4 GHz antennas.
- Maintain at least 20 mm clearance between antenna elements and metal structures to avoid de-tuning.
- Run antenna cables away from switching power supplies, clock oscillators, and high-speed digital traces.
- Perform antenna impedance matching (50 Ω) and RF trace design in compliance with local regulatory requirements.

7.4 Reset Circuit

- The WSB530 has an internal voltage monitor that controls reset automatically. For applications requiring external reset capability, connect a push-button or supervisor IC to PQ_RSTIN_N.
- PQ_RSTIN_N is active low. Add a 10 k Ω pull-up resistor to 3.3 V and a 100 nF debounce capacitor if using a mechanical push-button.
- Ensure the reset signal is not toggled during normal operation to avoid unexpected module restarts.

8. Configuration

The WSB530 runs an OpenWrt 23.05-based firmware stack. Configuration access depends on the carrier board implementation — the carrier board must provide at least one of the following access methods.

8.1 Default Settings

The following figure provides a basic system-level overview of the WSB530 module and its connection to a host CPU/SoC platform.

Default Management IP	192.168.1.1 (when Ethernet PHY and interface are configured)
Default Subnet	192.168.1.0/24
WebUI Port	80 (HTTP) / 443 (HTTPS)
Default Username	admin
Default Password	password
SSH Access	Port 22 (enabled by default)
UART Baud Rate	115200 bps, 8N1
Default Mode	Router / Access Point
Firmware	OpenWrt 23.05

8.2 Serial Console Access

Serial console access via UART is the recommended primary access method during development, as it does not depend on carrier board Ethernet implementation.

- Connect a TTL serial converter to the UART pins exposed on the carrier board.
- Configure the serial terminal: 115200 bps, 8N1, no flow control.
- Serial console provides full OpenWrt shell access for firmware configuration and debugging.

8.3 Wireless Configuration

Wireless settings can be configured via webUI, OpenWrt UCI commands or by editing configuration files directly via serial console or SSH.

- Via Web User Interface (webUI): Navigate to Network > Wireless to configure SSIDs, security, channels, and transmit power for each band.
- Via SSH: Connect using PuTTY or any SSH client, entering the IP address 192.168.1.1 and port 22.
- Via Serial Console: Connect using TeraTerm with the 4-pin TTL serial header (115200 bps, 8N1) and a TTL serial converter.
- Wireless configuration files are located at /etc/config/wireless.
- Use UCI commands to modify wireless settings, for example:

```
uci set wireless.wifi0.disabled='0'
```

```
uci set wireless.wifi0.htmode='EHT40'
```

```
uci commit wireless
```

```
wifi
```

- Use iw dev to verify radio status after applying changes.

9. Troubleshooting

The following table covers common integration issues. As the WSB530 is a SoM, most issues are related to carrier board design or interface implementation.

Module does not power on	Verify all three power rails (12 V, 5 V, 3.3 V) are present and within spec at the edge connector pads. Confirm all GND pins are connected. Check power sequencing.
No UART output	Verify UART pins are correctly connected on the carrier board. Confirm terminal is set to 115200 bps, 8N1. Check TTL level compatibility of serial converter.
No Ethernet connectivity	Verify Ethernet PHY is correctly connected to USXGMII (pins 101–114). Check PHY power, reset, and MDC/MDIO (GPIO_27/GPIO_28) connections. Confirm PHY driver is loaded in firmware.
2.4 GHz SSID not visible	Verify 2.4 GHz antennas are connected to both U.FL ports (CH0, CH1). Confirm module has completed boot. Use <code>iw dev</code> or <code>uci show wireless</code> to verify radio is enabled.
PCIe device not detected	Check PCIe trace routing on carrier board (impedance, length matching, AC coupling). Verify PCIe power and reset signals (pins 11–16). Confirm PCIe lane configuration (1L vs 2L).
USB device not detected	Verify USB mode (Option 1 = USB 3.0, Option 2 = USB 2.0 + PCIe). Check USB trace routing and carrier board implementation.
Module overheating	Ensure adequate airflow and thermal management on the carrier board. Add a heatsink to the SoC if required. Verify ambient temperature is within the rated operating range.
Unexpected resets	Check power supply stability — voltage dips during load transients may trigger the voltage monitor reset. Improve bulk capacitance and regulator transient response on carrier board.
Firmware upgrade fails	Use UART serial console for initial firmware recovery. Ensure stable power during upgrade. Do not interrupt the process once started.
Factory Reset	To restore factory default settings via UART serial console or SSH: <code>rm -rf /overlay/*</code> <code>reboot</code> The module will reboot and restore all settings to factory defaults within approximately 60 seconds.

10. Safety Precautions

Electrical Safety

- Disconnect power from the carrier board before making any connections or modifications to the hardware.
- Never exceed the rated input voltages (12 V, 5 V, 3.3 V) on any power rail. Overvoltage will permanently damage the module.
- Carrier board power supply design must include adequate protection (OVP, OCP) on all input rails.
- Ensure all GND pins on the edge connector are connected to carrier board ground before applying power.

RF / Antenna Safety

- Never power on the WSB530 with the 2.4 GHz radio active and U.FL ports left open (unterminated). Connect antennas or 50 Ω loads before applying power.
- Maintain a minimum safety distance of 20 cm from all active antennas during normal operation.
- For 6 GHz operation, ensure all required regulatory approvals are obtained for the target market.
- Do not modify the RF circuitry or U.FL connectors on the WSB530 module.

Thermal Safety

- The WSB530 module and SoC may reach elevated temperatures during operation, particularly under high RF throughput. Ensure the carrier board design includes adequate thermal management (heatsinking, airflow, thermal interface materials).
- Do not operate beyond the rated temperature range. Thermal shutdown may occur to protect the SoC.

ESD Precautions

- Handle the WSB530 only at a properly grounded ESD workstation.
- Wear an ESD wrist strap at all times when handling the module.
- Store the WSB530 in its original ESD protective bag when not in use.
- Avoid touching the stamp-hole edge connector pads or any exposed PCB traces directly.

11. Technical Support

Compex Systems Pte Ltd provides engineering and technical support for the WSB530. For technical assistance, integration support, or to report a hardware issue, please contact:

Company	Compex Systems Pte Ltd
Headquarters	Singapore
Sales Enquiries	sales@compex.com.sg
Technical Support	https://compex.com.sg/support-downloads/
Website	https://compex.com.sg
Product Page (WSB530)	https://compex.com.sg/shop/embedded-board/802-11be-embedded-board/wsb530-ginger-wifi7-som/
Qualcomm Design Centre	Qualcomm Authorized Design Centre (ADC) since 2014

Before contacting support, please:

- Review this user guide, the WSB530 Hardware Design Guide, and the Troubleshooting section (Section 9).
- Note the firmware version (via UART serial console: `cat /etc/openwrt_release`).
- Provide carrier board schematics and PCB layout files relevant to the reported issue.
- Describe the issue with steps to reproduce, observed symptoms, and test conditions.

For sample requests, pre-production evaluations, or OEM/ODM partnership enquiries, contact the Compex sales team at sales@compex.com.sg.

12. Full Specifications

Model Number	WSB530 (Codename: GINGER)
SoC	Qualcomm IPQ5322 ‘Miami’ Series, Quad-Core ARM Cortex-A53 @ 1.5 GHz
Reference Design	Qualcomm AP.MI01.2
System Memory	1 GB DDR4 (up to 3 GB), 16-bit interface (1× 16-bit)
NOR Flash	None
eMMC Flash	16 GB
On-Board Wi-Fi	2×2 MU-MIMO 802.11b/g/n/ax/be (2.4 GHz), max 22 dBm per chain; up to 688 Mbps
Wi-Fi Standard	IEEE 802.11be (Wi-Fi 7) — backward compatible to 802.11a/b/g/n/ac/ax
Frequency Range	2.4 GHz: 2.412–2.472 GHz
Channel Widths	2.4 GHz: 20/40 MHz (EHT20 / EHT40)
Modulation	OFDMA: BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM, 4096-QAM
RF Connectors (On-Module)	2× U.FL (IPEX1) for 2.4 GHz (CH0, CH1)
PCIe 3.0	2× PCIe 3.0
USB	1× USB 3.0 (or 1× USB 2.0 + 1L PCIe 3.0 option)
BLSP / Serial	3× BLSP ports (UART, I2C, SPI)
GPIOs	33× GPIOs — exposed via 150-pin edge connector
PWM	4× PWM outputs — exposed via 150-pin edge connector
Ethernet	2× multi-GbE Ethernet SerDes (USXGMII); external PHY required on carrier board
Edge Connector	150-pin stamp-hole connector (underside of module)
Power Input	12 V (DVDD_12V), 5 V (5V_in), 3.3 V (DVDD_3V3) — all supplied from carrier board via 150-pin edge connector
Max Power Consumption	6 W (module only, excluding carrier board and peripherals)
Reset	Via on-module voltage monitor; external reset via PQ_RSTIN_N (pin 137, active-low)
Dimensions (W×H×D)	65 mm × 45 mm × 7.4 mm

Humidity	5–95% non-condensing (operating); Max 90% (storage)
OS / Firmware	OpenWrt 23.05
SDK	SDKs with QCA binary drivers available for software developers
Accessories	JTAG Programmer, Serial Converter, Power Supply (if available)
Certification	CE Certified, REACH & RoHS Compliant
Ordering Code (Sample)	WSB530 6A02BW0F1GB-TE
Ordering Code (Mass Production)	WSB530 6A02BW0F1GB

13. Regulatory Information

Declaration of Conformity

The WSB530 is designed to comply with applicable regional regulatory requirements. The WSB530 is a component-level SoM intended for integration into end products. End-product manufacturers are responsible for obtaining all necessary regulatory certifications (e.g., FCC, CE, IMDA) for their final product in each target market, including any additional certifications required for the complete carrier board assembly.

6GHz Band Restrictions

Operation in the 6 GHz frequency band is subject to national regulatory authority approval. Manufacturers must ensure compliance with local regulations before enabling 6 GHz radio operation in their end product.

REACH & RoHS Compliance

This product is manufactured in compliance with REACH Regulation (EC) No 1907/2006 and RoHS Directive 2011/65/EU (amended by 2015/863/EU), restricting the use of hazardous substances in electrical and electronic equipment.

Disposal & Recycling

Do not dispose of this product in unsorted municipal waste. This product is subject to the Waste Electrical and Electronic Equipment (WEEE) Directive. At the end of its service life, return the product to an authorized recycling facility or contact Compex Systems for take-back options.

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